# AIM

# Comparative study and making of Full 4-bit adder circuit.

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# ADDER

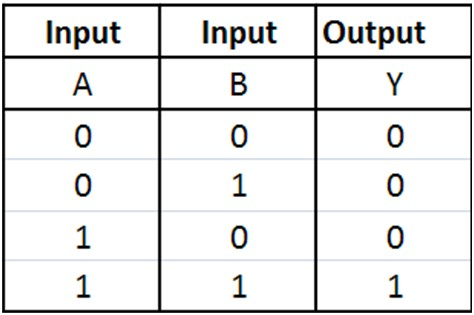
In electronics, an adder or summer is a digital circuit that performs addition of numbers. In many computers and other kinds of processors, adders are used not only in the arithmetic logic units, but also in other parts of the processor, where they are used to calculate addresses, table indices, increment and decrement operators, and similar operations.

Although adders can be constructed for many numerical representations, such as binary-coded decimal or excess-3, the most common adders operate on binary numbers. In cases where two's complement or ones' complement is being used to represent negative numbers, it is trivial to modify an adder into an adder– subtractor. Other signed number representations require more logic around the basic adder.

**AND GATE**

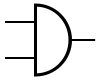
The AND gate is a basic digital logic gate that implements logical conjunction - it behaves according to the truth table below. A HIGH output

1. Results only if both the inputs to the AND gate are HIGH (1). If neither or only one input to the AND gate is HIGH, a LOW output results. In another sense, the function of AND effectively finds the minimum between two binary digits, just as the OR function finds the maximum. Therefore, the output is always 0 except when all the inputs are 1.



#### SYMBOLS

There are three symbols for AND gates: the American (ANSI or 'military') symbol and the IEC ('European' or 'rectangular') symbol, as well as the deprecated DIN symbol.



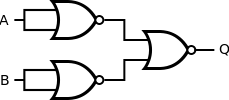
*MIL/ANSI Symbol IEC Symbol DIN Symbol*

The AND gate with inputs *A* and *B* and output *C* implements the logical expression **C = A.**

#### ALTERNATIVES

If no specific AND gates are available, one can be made from NAND or NOR gates, because NAND and NOR gates are considered the "universal gates," meaning that they can be used to make all the others.

**Desired gate NAND construction NOR construction**



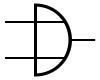
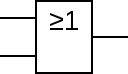
### OR GATE

The OR gate is a digital logic gate that implements logical disjunction - it behaves according to the truth table below. A HIGH output (1) results if one or both the inputs to the gate are HIGH (1). If neither input is high, a LOW output (0) results. In another sense, the function of OR effectively finds the maximum between two binary digits, just as the complementary AND function finds the minimum.

|  |  |  |
| --- | --- | --- |
| **INPUT** | | **OUTPUT** |
| A | B | A OR B |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

#### SYMBOLS

There are two symbols of OR gates: the American (ANSI or 'military') symbol and the IEC ('European' or 'rectangular') symbol, as well as the deprecated DIN symbol.

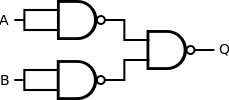


*MIL/ANSI Symbol IEC Symbol DIN Symbol*

#### ALTERNATIVES

If no specific OR gates are available, one can be made from NAND or NOR gates in the configuration shown in the image below. Any logic gate can be made from a combination of NAND or NOR gates.

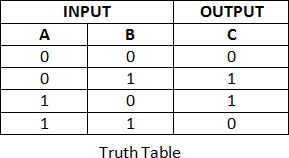
**NAND Construction NOR construction**



### XOR GATE

The XOR gate (sometimes EOR gate, or EXOR gate and pronounced as Exclusive OR gate) is a digital logic gate that implements an exclusive or; that is, a true output (1/HIGH) results if one, and only one, of the inputs to the gate is true. If both inputs are false (0/LOW) or both are true, a false output results. XOR represents the inequality function, i.e., the output is true if the inputs are not alike otherwise the output is false. A way to remember XOR is "one or the other but not both".

XOR can also be viewed as addition modulo 2. As a result, XOR gates are used to implement binary addition in computers. A Half adder consists of an XOR gate and an AND gate. Other uses include subtractors, comparators, and controlled inverters.



The algebraic expressions A.B' + B.A' and (A+B).(A'+B') both represent the XOR gate with inputs *A* and *B*. The behavior of XOR is summarized in the truth table shown on the right.

#### SYMBOLS

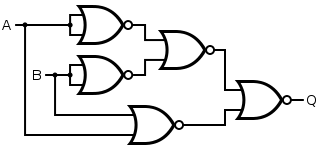
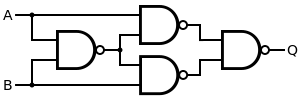
There are two symbols for XOR gates: the traditional symbol and the IEEE symbol



Traditional XOR Symbol IEEE XOR Symbol

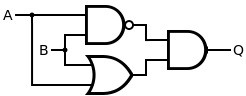
#### ALTERNATIVES

If a specific type of gate is not available, a circuit that implements the same function can be constructed from other available gates. A circuit implementing an XOR function can be trivially constructed from an XNOR gate followed by a NOT gate. If we consider the expression A.B'+A'.B , we can construct an XOR gate circuit directly using AND, OR and NOT gates. An XOR gate circuit can also be made from four NAND or five NOR gates in the configuration shown below.



XOR gate circuit constructed using only XOR gate circuit constructed using only

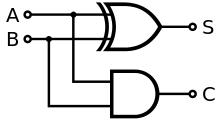
NAND gates. NOR gates.



XOR gate circuit using three mixed gates.

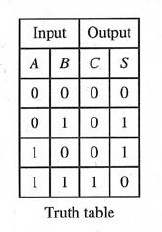
### HALF ADDER

The half adder adds two single binary digits A and B. It has two outputs, sum (S) and carry (C). The carry signal represents an overflow into the next digit of a multi-digit addition. The value of the sum is 2C + S. The simplest half-adder design, pictured on the right, incorporates an XOR gate for S and an AND gate for C. With the addition of an OR gate to combine their carry outputs, two half adders can be combined to make a full adder.

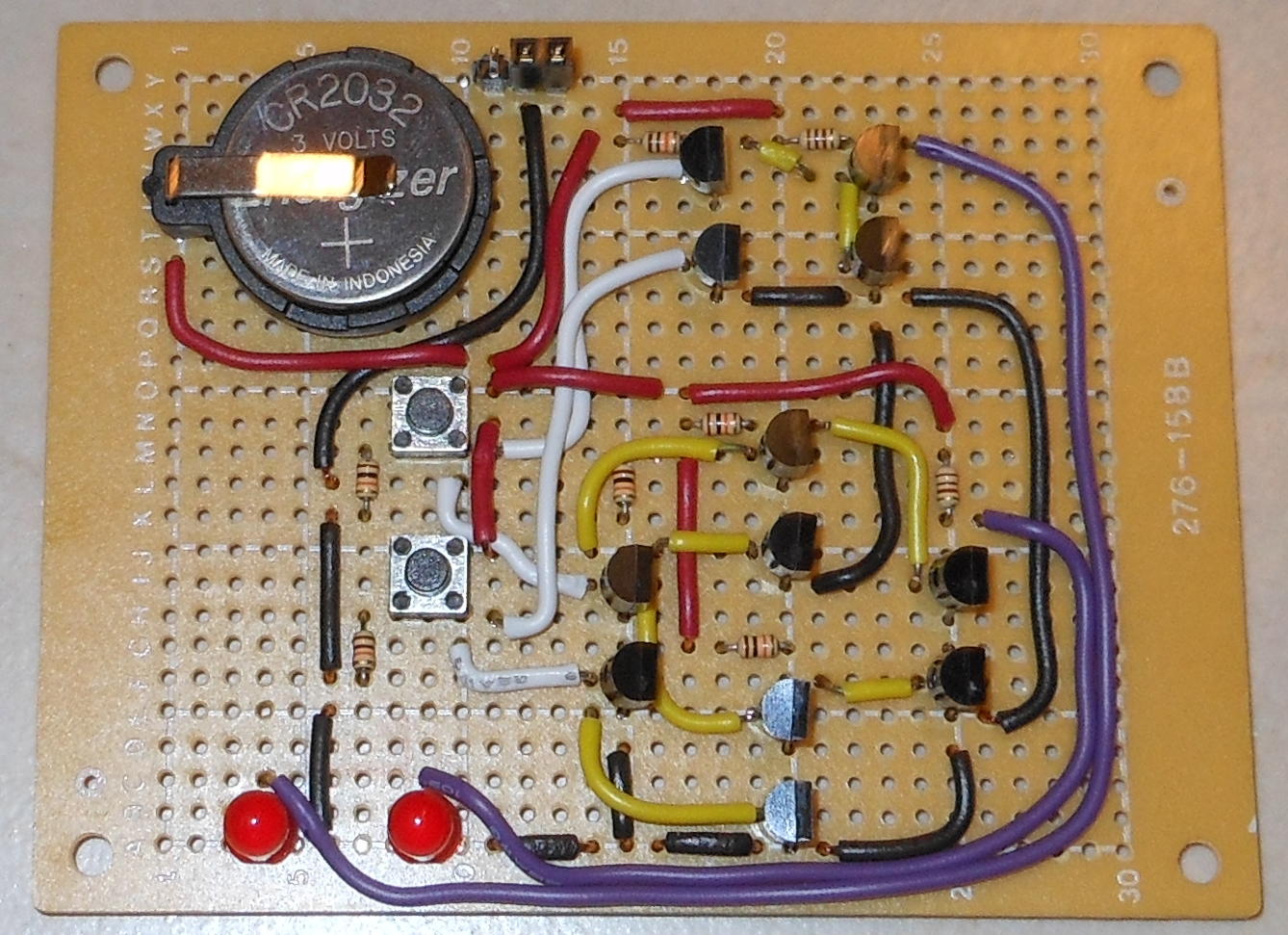


Half adder logic diagram

The half adder adds two input bits and generates a carry and sum, which are the two outputs of a half adder. The input variables of a half adder are called the augend and addend bits. The output variables are the sum and carry. The truth table for the half adder is:

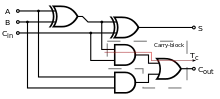


(IMAGE OF HALF BIT ADDER USING TRANSISTORS)



### FULL ADDER

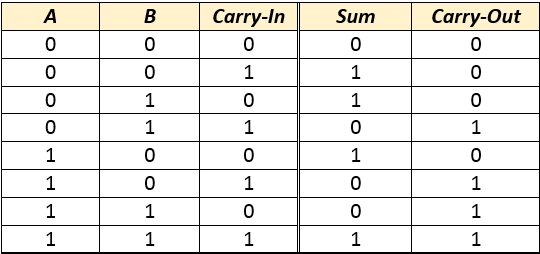
A full adder adds binary numbers and accounts for values carried in as well as out. A one-bit full adder adds three one-bit numbers, often written as *A*, *B*, and *C*in; *A* and *B* are the operands, and *C*in is a bit carried in from the previous less significant stage. The full adder is usually a component in a cascade of adders, which add 8, 16, 32, etc. bit binary numbers. The circuit produces a two-bit output, output carry and sum typically represented by the signals *C*out and *S*, where sum = 2*C*out + S.



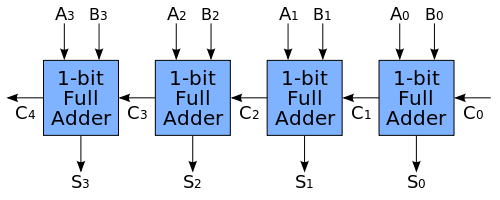
Schematic symbol for a 1-bit full adder Logic diagram for a full adder.

In this implementation, the final OR gate before the carry-out output may be replaced by an XOR gate without altering the resulting logic. Using only two types of gates is convenient if the circuit is being implemented using simple IC chips which contain only one gate type per chip.

A full adder can be constructed from two half adders by connecting *A* and *B* to the input of one half adder, connecting the sum from that to an input to the second adder, connecting *Ci* to the other input and OR the two carry outputs.



### RIPPLE CARRY ADDER

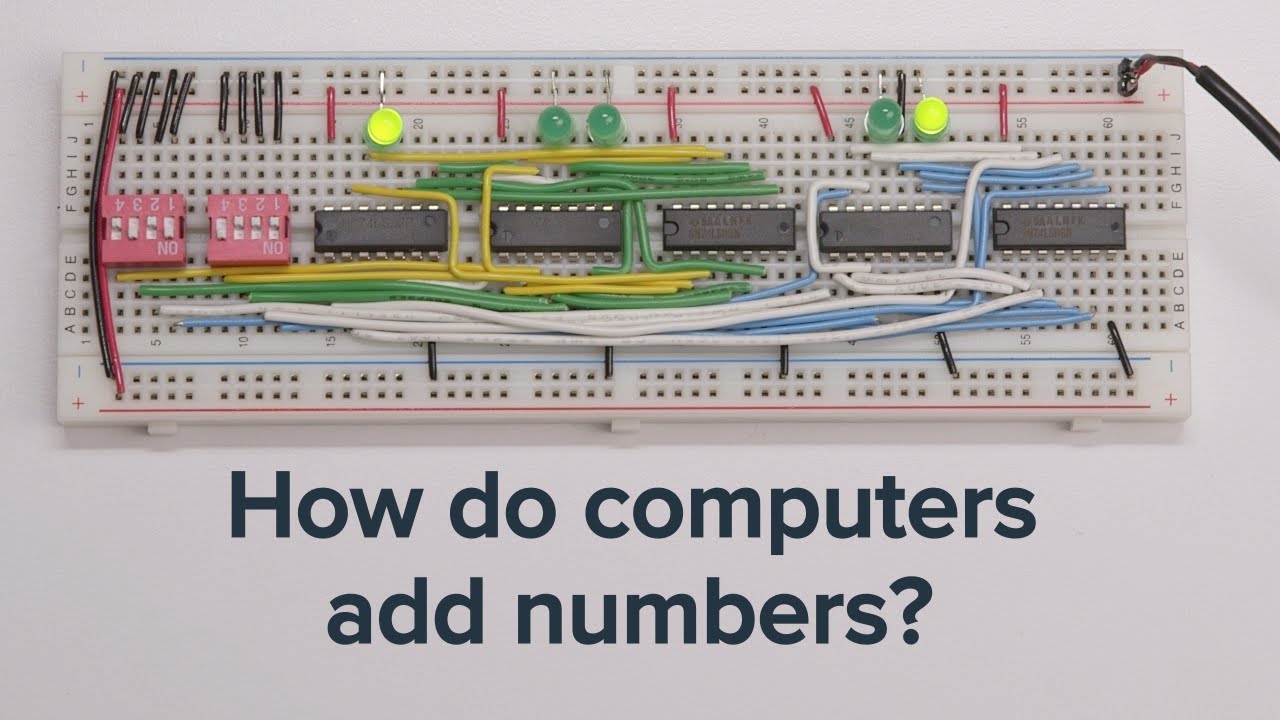


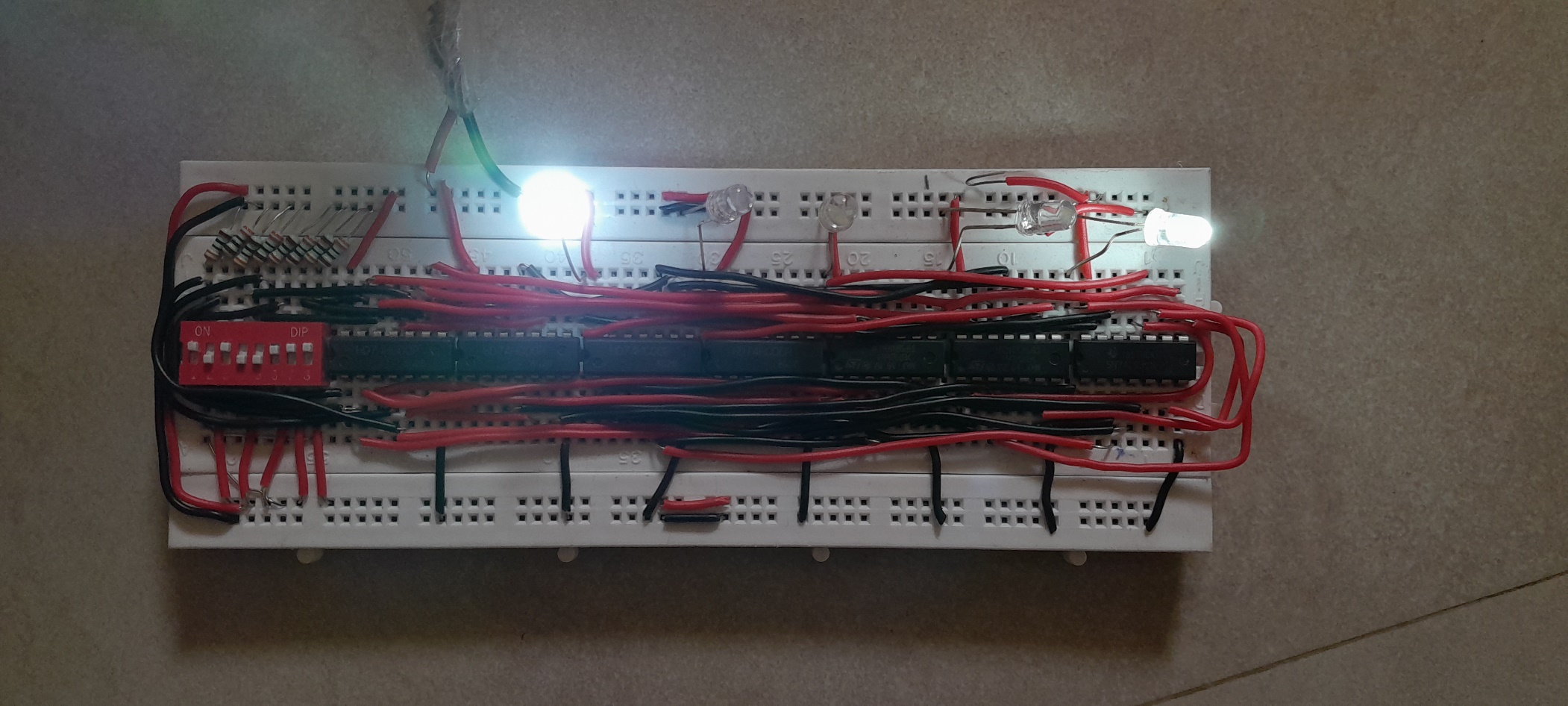
It is possible to create a logical circuit using multiple full adders to add *N*- bit numbers. Each full adder inputs a *Cin*, which is the *Cout* of the previous adder. This kind of adder is called a *ripple-carry adder*, since each carry bit "ripples" to the next full adder. Note that the first full adder may be replaced by a half adder (under the assumption that *Cin =0*).

The layout of a ripple-carry adder is simple, which allows for fast design time; however, the ripple-carry adder is relatively slow, since each full adder must wait for the carry bit to be calculated from the previous full adder. The gate

delay can easily be calculated by inspection of the full adder circuit. Each full adder requires three levels of logic. In a 4-bit ripple-carry adder, there are 4 full adders, so the critical path (worst case) delay is 3 (from input to carry in first adder) + 3 \* 2 (for carry propagation in later adders) = 9 gate delays.

(IMAGE OF FOUR BIT ADDER USING LOGIC GATE ICS)





# BIBLIOGRAPHY

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#### [www.wikipedia.com](http://www.wikipedia.com)

#### [www.youtube.com/c/BenEater](http://www.youtube.com/c/BenEater)

#### BOOKS

#### NCERT Physics Book (Class-XII)

#### Morris Mano Architecture